Remarks/Arguments

The Applicant thanks the Examiner for the interview provided by telephone on June 6, 2006. During the interview, Leitch (5,559,506) and Cantarella (4,417,339) were generally discussed as they related to claims 1 and 12. In particular, the Examiner and the Applicant's representative discussed whether Leitch and Cantarella described error detection occurring at two levels--both a bit-level and a byte-level, as recited in claim 1. The Examiner and the Applicant's representative also discussed the meaning of "byte". No agreement was reached.

Claims 1-23 were examined in the current Office Action. Claim 12 has been amended to include the recitations of claim 14. Claim 14 has been cancelled, and claim 15 has been amended to depend from claim 12 rather than claim 14. No other amendments have been made; no other claims have been cancelled; and no claims have been added. Because the amendments to the claims do not introduce new recitations, no further search is needed. Accordingly, Applicant respectfully submits that the present amendments should be entered, and requests that claims 1-13 and 15-23 be considered in light of the remarks below. Claims 1 and 12 are independent.

Claims 1-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Leitch in view of Cantarella. The Applicant respectfully traverses the rejection because the Office Action has not found all of the claimed recitations in the applied art.

Claims 1 and 12 each recite three separate coding or error detection operations. Claim 1 recites three error detection operations as follows (emphasis added):

(1) "performing a parity check for each one of said N rows of said data block ... [for detecting bit-level errors],"

(2) "performing a parity check for each one of said X columns of said data block ... for detecting bit-level errors," and

(3) "identifying at least one bad byte for said data block using a byte-level error detection process."

These are three distinct, separate operations, and all three must be found in the applied art if the claim is to be rejected. That these are three distinct, separate operations is further indicated by the fact that the "identifying" operation references all three of the encoding operations. These references are indicated by the underlining in the following quote from claim 1: "identifying, from said parity check for each one of said N rows of said

data block, from said parity check for each one of said X columns of said data block and from said at least one identified bad bytes for said data block [identified using the byte-level error detection process], at least one error in said data block" (claim 1, emphasis added).

Leitch does not describe or suggest a process with three separate, distinct error detection operations as recited in claim 1. Rather, Leitch describes a matrix process that checks the parity for the rows in the matrix (referred to as a tier), checks the parity for the columns in the matrix, and then uses the results of the two parity checking operations to determine the individual errors in the matrix (see, e.g., Leitch at col. 14, line 53 - col. 15, line 22).

Even if Leitch's two parity checks are equated with claim 1's two parity checking operations for detecting bit-level errors, Leitch does not describe a separate third error detection operation. Moreover, Leitch does not describe a separate third error detection operation that operates on a byte-level. Although the Examiner adopts a broad definition of "byte," even a broad definition of "byte" must define a "byte" to be larger than a "bit." Accordingly, even if a separate, third error detection operation were taught by Leitch, such an operation would have to be a "byte-level error detection process" (claim 1) and would have to operate on a larger group of data than the recited "parity check[s] ... for detecting bit-level errors" (claim 1).

Cantarella describes a parity-coding process that operates on bits, and Cantarella is cited in the Office Action to provide a teaching of determining bit-level errors. More particularly, Cantarella appears to be applied by the Office Action in order to suggest that the "symbols" of Leitch's tiers could be bits. Even accepting such a combination, it is clear that the applied portions of Cantarella are not cited to provide a third encoding operation, and indeed do not describe a third encoding operation as recited. Accordingly, Cantarella is not cited by the Office Action to cure, and does not cure, the deficiencies of Leitch identified above.

For at least the above reasons, claim 1 and all claims depending from claim 1 are patentable over the applied references. Accordingly, the Applicant respectfully requests allowance of these claims.

Claim 12 similarly includes recitations referring to three separate, distinct operations. Although claim 12 is similar to claim 1, there is a contrast in that claim 12

specifically refers to "encoding" operations rather than error detection operations as in claim 1. These operations are indicated by the following underlining:

> [W]herein said confirmed error bits are identified using a combination of information derived from 8B/10B encoding of said data block, information derived from parity encoding along each row of said data block and information derived from parity encoding along each column of said data block.

(Claim 12, emphasis added.) Thus, claim 12 recites the three separate, distinct encoding operations of (1) 8B/10B encoding of the block, (2) parity encoding along each row of the block, and (3) parity encoding along each column of the block. As explained above for claim 1, Leitch does not disclose or suggest three separate error detection operations. Similarly, Leitch does not disclose or suggest three separate encoding operations. Rather, Leitch merely provides a parity encoding of the rows of a tier, and a parity encoding of the columns of a tier. Leitch does not describe a third encoding, much less a third encoding that is an 8B/10B encoding of a data block.

In rejecting now-cancelled claim 14, the Office Action acknowledges that "Leitch does not explicitly teach 8B/10B" (Office Action at page 9). The Office Action then asserts that "Leitch teaches (Q + S) bits of data wherein Q equals 4 and S equals 2" and that it would have been obvious "to realize that Leitch's Q could equal to 8 and S could equal to 2" (Office Action at page 9). The Office Action thus proposes to modify Leitch's row-parity checking operation to use 8 data symbols (not described as bits in Leitch) and 2 parity symbols. However, such a modification would only impact Leitch's existing parity-checking operation. Such a modification would not provide a third encoding operation. Accordingly, even accepting the modification, the Office Action has not shown three separate encoding operations in Leitch.

For at least the above reasons, claim 12 and all claims depending from claim 12 are patentable over the applied references. Accordingly, the Applicant respectfully requests allowance of these claims.

If the Examiner would find a telephone discussion to be of value in advancing the prosecution of this case, the Examiner is invited to contact the Applicant's attorney at (609) 734-6817.

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No fees are believed to be due. However, any necessary fees may be charged, and any credits may be applied, to Deposit Acct. No. 07-0832.

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I hereby certify that this correspondence is being transmitted via facsimile to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 2313-1450 on June 7, 2006 at facsimile number (571) 273-8300.